

What Is Claimed Is:

1 1. A shift-register unit, comprising:
2 a first transistor having a first source/drain coupled to
3 a first terminal, a second source/drain, and a first
4 gate coupled to a reset signal to stop the
5 shift-register unit outputting a pulse signal;
6 a second transistor having a third source/drain coupled to
7 the second source/drain, a fourth source/drain
8 coupled to a second terminal, and a second gate
9 coupled to a setting signal to the initial
10 shift-register unit;
11 a third transistor having a fifth source/drain coupled to
12 an output terminal, a third gate coupled to the second
13 source/drain and a sixth source/drain coupled to a
14 clock signal to start outputting the pulse signal;
15 and
16 a fourth transistor having a seventh source/drain coupled
17 to the first terminal, an eighth source/drain coupled
18 to the output terminal and a fourth gate coupled to
19 a refresh signal to set a voltage level of the
20 shift-register unit in a standby mode.

1 2. The shift-register unit as claimed in claim 1, further
2 comprising a fifth transistor having a ninth source/drain
3 coupled to the first terminal, a tenth source/drain coupled to
4 the second source/drain and a fifth gate coupled to a preset
5 signal to set a voltage level of the third gate.

1 3. The shift-register unit as claimed in claim 2, wherein
2 the transistors are p-type transistors and the first terminal

3 is coupled to a power source and the second terminal is coupled
4 to the setting signal.

1 4. The shift-register unit as claimed in claim 2, wherein
2 the transistors are p-type transistors and the voltage level of
3 the first terminal exceeds that of the second terminal.

1 5. The shift-register unit as claimed in claim 2, wherein
2 the transistors are n-type transistors and the first terminal
3 is coupled to a ground level and the second terminal is coupled
4 to the setting signal.

1 6. The shift-register unit as claimed in claim 2, wherein
2 the transistors are n-type transistors and the voltage level of
3 the second terminal exceeds that of the first terminal.

1 7. The shift-register unit as claimed in claim 1, wherein
2 the transistors are thin film transistors.

1 8. The shift-register unit as claimed in claim 1, wherein
2 the transistors are MOS transistors.

1 9. A shift-register circuit, comprising:

2 a first-stage shift-register unit, a final-stage
3 shift-register unit and a plurality of middle-stage
4 shift-register units connected between the
5 first-stage shift-register unit and the final-stage
6 shift-register unit, wherein the shift-register
7 units are connected in serial and each shift-register
8 unit outputs a pulse signal in sequence after the
9 first-stage shift-register unit receives an initial
10 setting signal;

11 each shift-register unit comprising:
12 a clock terminal for receiving a clock signal;
13 a setting terminal for receiving a setting signal for
14 triggering the shift-register unit to output the
15 clock signal as the pulse signal; and
16 a reset terminal for receiving a reset signal to
17 reset the shift-register unit to stop
18 outputting the pulse signal, wherein the reset
19 terminals of the first-stage and the
20 middle-stage shift-register units are
21 respectively connected to the output signal of
22 the subsequent stage shift-register unit, the
23 reset terminal of the final-stage
24 shift-register unit is connected to the output
25 signal of the first-stage shift-register unit,
26 the setting terminal of the middle-stage and
27 the final-stage shift-register units are
28 respectively connected to the output signal of
29 the previous stage shift-register unit, the
30 setting terminal of the first-stage
31 shift-register unit is connected to the initial
32 setting signal, the clock terminals of the odd
33 stage shift-register units are connected to a
34 first clock signal as the clock signal and the
35 clock terminals of the even stage
36 shift-register units are connected to a second
37 clock signal as the clock signal.

1 10. The shift-register circuit as claimed in claim 9,
2 wherein the shift-register unit comprises:

3 a first transistor having a first source/drain coupled to
4 a first terminal, a second source/drain, and a first
5 gate coupled to the reset terminal;
6 a second transistor having a third source/drain coupled to
7 the second source/drain, a fourth source/drain
8 coupled to a second terminal, and a second gate as
9 the setting terminal; and
10 a third transistor having a fifth source/drain coupled to
11 an output terminal, a third gate coupled to the second
12 source/drain and a sixth source/drain as the clock
13 terminal.

1 11. The shift-register circuit as claimed in claim 10,
2 wherein the shift-register unit further comprises:

3 a fourth transistor having a seventh source/drain coupled
4 to the first terminal, an eighth source/drain coupled
5 to the output terminal and a fourth gate as a refresh
6 terminal coupled to a refresh signal to set a voltage
7 level of the shift-register unit in a standby mode;
8 and
9 a fifth transistor having a ninth source/drain coupled to
10 the first terminal, a tenth source/drain coupled to
11 the second source/drain and a fifth gate as a preset
12 terminal to set a voltage level of the third gate,
13 wherein the refresh terminals of the even stage
14 shift-register units are coupled to the first clock
15 signal, and the refresh terminals of the odd stage
16 shift-register units are coupled to the second clock
17 signal.

1 12. The shift-register circuit as claimed in claim 11,
2 wherein the first and the second clock signals have the same
3 frequency and different duty cycles.

1 13. The shift-register circuit as claimed in claim 12,
2 wherein the transistors are p-type transistors and the first
3 terminal is coupled to a power source and the second terminal
4 is coupled to the setting signal.

1 14. The shift-register unit as claimed in claim 12,
2 wherein the transistors are p-type transistors and the voltage
3 level of the first terminal exceeds that of the second terminal.

1 15. The shift-register unit as claimed in claim 12,
2 wherein the transistors are n-type transistors and the first
3 terminal is coupled to a ground level and the second terminal
4 is coupled to the setting signal.

1 16. The shift-register unit as claimed in claim 12,
2 wherein the transistors are n-type transistors and the voltage
3 level of the second terminal exceeds that of the first terminal.

1 17. The shift-register unit as claimed in claim 10,
2 wherein the transistors are thin film transistors.

1 18. The shift-register unit as claimed in claim 10,
2 wherein the transistors are MOS transistors.

1 19. A shift-register circuit, comprising:
2 a first-stage shift-register unit, a second-stage
3 shift-register unit, a third-stage shift-register
4 unit and a fourth-stage shift-register unit

5 connected in serial, wherein each shift-register
6 unit outputs a pulse signal in sequence after the
7 first-stage shift-register unit receives an initial
8 setting signal;

9 each shift-register unit comprising:

10 a clock terminal for receiving a clock signal;

11 a setting terminal for receiving a setting signal for
12 triggering the shift-register unit to output
13 the clock signal as the pulse signal; and

14 a reset terminal for receiving a reset signal to
15 reset the shift-register unit to stop

16 outputting the pulse signal, wherein the reset

17 terminals of the first-stage, the second-stage

18 and the third-stage shift-register units are

19 respectively connected to the output signal of

20 the subsequent stage shift-register unit, the

21 setting terminal of the second-stage, the

22 third-stage and the fourth stage

23 shift-register units are respectively

24 connected to the output signal of the previous

25 stage shift-register unit, the setting

26 terminal of the first-stage shift-register

27 unit is connected to the initial setting

28 signal, the clock terminals of the first-stage

29 and the fourth-stage shift-register units are

30 connected to a first clock signal as the clock

31 signal, the clock terminal of the second-stage

32 shift-register unit is connected to a second

33 clock signal as the clock signal and the clock

34 terminal of the third-stage shift-register

unit is connected to a third clock signal as the
clock signal.

20. The shift-register circuit as claimed in claim 19,
wherein the shift-register unit comprises:

a first transistor having a first source/drain coupled to
a first terminal, a second source/drain, and a first
gate coupled to the reset terminal;

a second transistor having a third source/drain coupled to
the second source/drain, a fourth source/drain
coupled to a second terminal, and a second gate as
the setting terminal; and

a third transistor having a fifth source/drain coupled to
an output terminal, a third gate coupled to the second
source/drain and a sixth source/drain as the clock
terminal.

21. The shift-register circuit as claimed in claim 20,
wherein the shift-register unit further comprises:

a fourth transistor having a seventh source/drain coupled
to the first terminal, an eighth source/drain coupled
to the output terminal and a fourth gate as a refresh
terminal coupled to a refresh signal to set a voltage
level of the shift-register unit in a standby mode;
and

a fifth transistor having a ninth source/drain coupled to
the first terminal, a tenth source/drain coupled to
the second source/drain and a fifth gate as a preset
terminal to set a voltage level of the third gate,
wherein the refresh terminal of the first-stage

14 shift-register unit is coupled to the first clock
15 signal, the refresh terminal of the second-stage
16 shift-register unit is coupled to the second clock
17 signal and the refresh terminal of the third-stage
18 shift-register unit is coupled to the third clock
19 signal.

1 22. The shift-register circuit as claimed in claim 21,
2 wherein the first, the second and the third clock signals have
3 the same frequency and different duty cycles.

1 23. The shift-register circuit as claimed in claim 22,
2 wherein the transistors are p-type transistors and the first
3 terminal is coupled to a power source and the second terminal
4 is coupled to the setting signal.

1 24. The shift-register unit as claimed in claim 22,
2 wherein the transistors are p-type transistors and the voltage
3 level of the first terminal exceeds that of the second terminal.

1 25. The shift-register unit as claimed in claim 22,
2 wherein the transistors are n-type transistors and the first
3 terminal is coupled to a ground level and the second terminal
4 is coupled to the setting signal.

1 26. The shift-register unit as claimed in claim 22,
2 wherein the transistors are n-type transistors and the voltage
3 level of the second terminal exceeds that of the first terminal.

1 27. The shift-register unit as claimed in claim 20,
2 wherein the transistors are thin film transistors.

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- 1 28. The shift-register unit as claimed in claim 20,
- 2 wherein the transistors are MOS transistors.